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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,855	02/24/2004	Soo-Bong Chang	8750-058	3631
20575	7590	11/10/2005	EXAMINER	
MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204				PHAN, TRONG Q
ART UNIT		PAPER NUMBER		
2827				

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/786,855	CHANG ET AL.
	Examiner	Art Unit
	TRONG PHAN	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 06 October 2005.  
 2a) This action is FINAL. 2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-15 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_

***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the an internal voltage generating circuit arranged on both the first and second side of the memory array as recited in lines 9-10 of claim 1. (It should be noted that there are two internal voltage generating circuits 20 and 30 arranged on both sides of the memory array 10 in Fig. 3 of the present invention) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear how an internal voltage generating circuit can be arranged on both the first and a second side of the memory array. It should be noted that there are two internal voltage generating circuits 20 and 30 arranged on both sides of the memory array 10 in fig. 3 of the present invention.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-15 are, insofar as definite, rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai, 6,385,115, in view of Kitade et al., 6,314,035.

Nakai, 6,385,115, discloses in Fig. 1 a memory device comprising:  
a memory cell array including memory cell blocks MB;  
active sense amplifier power supply control circuit 1a and 1b arranged respectively on both sides of memory cell array, as shown in Fig. 2, each configured to compare

reference voltage  $V_{ref1}$  with an internal voltage  $V_{int}$  to generating a comparing signal which is also  $V_{int}$ ;

power supply driver 3a and 3b arranged respectively on both ends of internal voltage generating lines SPL to supply internal voltage VCCA to internal voltage generating lines SPL as shown in Fig. 4;

external voltage pads  $V_{ext}$ ;

column selection circuit (not shown) (see lines 5-9, column 4).

What is not shown in Nakai, 6,385,115, is the column decoder circuit comprising: a column address buffer, a column address pre-decoder and column selecting driving circuits as recited in claim 5.

Kitade et al., 6,314,035, discloses in Fig. 2 the teaching of using an address buffer 24, column predecoder 28 and column decoder 100 for driving column selecting lines CSL of the memory cell array MCB.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the column decoder circuit in Fig. 2 of Kitade et al., 6,314,035, for the column selection circuit (not shown) in Nakai, 6,385,115 for the purpose of capable applying a stress voltage to a column select line and capable of manifest a short-circuit failure associated with the column select line (see the summary of the invention of Kitade et al., 6,314,035. Arraging power supply drivers 3b between the column selecting lines as recited in claim 5 would have also been obvious to one of ordinary skill in the art since it is merely a matter of design choice for the compactness of the device.

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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HOAI HO can be reached on (571)272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*phanTrong*

TRONG PHAN  
PRIMARY EXAMINER